Amendments to the Claims

Listing of Claims:

Claims 1 - 10 (canceled).

Claim 11 (new). A device for equalizing a charge of serially connected capacitors belonging to a double layer capacitor, the double layer capacitor further having a positive terminal and a negative terminal, the device comprising:

a plurality of single diodes;

a switching transistor having a collector/drain terminal, a base/gate terminal and an emitter/source terminal;

a first diode;

a first resistor having a first terminal and a second terminal connected to the negative terminal of the double layer capacitor;

a second resistor;

a flyback transformer having a primary winding and a secondary winding wound in phase-opposition to one another, an end of winding of said primary winding connected to the positive terminal of the double layer capacitor and a start of said winding of said primary winding connected to said collector/drain terminal of said switching transistor, an end

of said secondary winding of said flyback transformer connected directly to the negative terminal of the double layer capacitor, a start of
said secondary winding connected by way of a series connection of said first diode and said second resistor to the negative terminal of the double layer capacitor;

a first voltage comparator having an inverting input connected to said emitter/source terminal of said switching transistor and to said first terminal of said first resistor, an output, and an noninverting input receiving a first reference voltage;

a first AND element having an output connected to said base/gate terminal of said switching transistor, first input receiving an external control signal, and a second input;

a second AND element having an output connected to said second input of said first AND element, a first input connected to said output of said first voltage comparator, and a second input;

a second voltage comparator having an inverting input connected to a connection point between said first diode and said second resistor, a noninverting input receiving the reference voltage, and an output connected to said second input of said second AND element;

a monitoring unit having a first input connected to said

output of said first voltage comparator, a second input connected to said output of said second voltage comparator, a third input connected to said inverting input of said second voltage comparator, a fourth input for receiving a second reference voltage, and an output outputting a status signal; and

a plurality of single transformers each being wound inphase and having a primary winding and a secondary winding, a start of said secondary winding of each of said single transformers connected through one of said single diodes to a positive terminal of a single one of said capacitors, and an end of said secondary winding in each case connected directly to a negative terminal of said single capacitor assigned to it, said primary winding of said single transformers connected in parallel with each other, and a common start of said primary winding connected to a connection point between said first diode and said second resistor and a common end of said primary winding connected to the negative terminal and to said end of said secondary winding of said flyback transformer.

Claim 12 (new). The device according to claim 11, wherein said single transformers and said single diodes are disposed together with the capacitors in a housing of the double layer capacitor.

Claim 13 (new). The device according to claim 11, further comprising a two-wire bus cable connecting said flyback

transformer to said single transformers.

Claim 14 (new). The device according to claim 11, further comprising a first capacitor having a first terminal connected to a cathode terminal of said first diode and a second terminal connected to the negative terminal.

Claim 15 (new). A device for equalizing a charge of serially connected capacitors belonging to a double layer capacitor, the double layer capacitor further having a positive terminal and a negative terminal, the device comprising:

a plurality of single diodes;

a switching transistor having a collector/drain terminal, a base/gate terminal and an emitter/source terminal;

a first diode;

a first resistor having a first terminal and a second terminal connected to the negative terminal of the double layer capacitor;

a second resistor having a first terminal and a second terminal connected to the negative terminal of the double layer capacitor;

a third resistor having a first terminal and a second terminal;

an inductor having a first terminal connected to the positive terminal of the double layer capacitor and a second terminal connected to said collector/drain terminal of said switching transistor,

a PNP transistor having a base terminal connected to said first terminal of said inductor, an emitter terminal connected through said third resistor and said first diode to said second terminal of said inductor, and a collector terminal connected through said second resistor to the negative terminal of the double layer capacitor;

a first voltage comparator having an inverting input connected both to said emitter/source terminal of said switching transistor and said first resistor, an non-inverting input for receiving a first reference voltage, and an output;

a first AND element having an output connected to said base/gate terminal of said switching transistor, a first input for receiving an external control signal, and a second input;

a second AND element having an output connected to said second input of said first AND element, a first input connected to said output of said first voltage comparator, and a second input;

a second voltage comparator having an inverting input connected to a connection point between said collector of said PNP transistor and said second resistor, a non-inverting input for receiving the first reference voltage, and an output connected to said second input of said second AND element;

a monitoring unit having a first input connected to said output of said first voltage comparator, a second input connected to said output of said second voltage comparator, a third input connected to said inverting input of said second voltage comparator, a fourth input for receiving a second reference voltage, and an output outputting a status signal; and

a plurality of single transformers each being wound in-phase, each of said single transformers having a secondary winding with a start of said secondary winding of each said single transformer being connected through one of said single diodes to the positive terminal of one of said capacitors, and an end of said secondary winding connected directly to the negative terminal of said capacitor, said single transformers having primary windings connected in parallel, said primary windings having a common start connected to a connection point between said first diode and said third resistor and a common end of said primary windings connected to the positive terminal of the double layer capacitor and to said first terminal of said inductor.

Claim 16 (new). The device according to claim 15, wherein said single transformers and said single diodes are disposed together with said capacitors in a housing of the double layer capacitor.

Claim 17 (new). The device according to claim 15, further comprising a two-wire bus cable connecting said inductor to said single transformers.

Claim 18 (new). The device according to claim 15, further comprising a first capacitor having a first terminal connected to a cathode terminal of said first diode and a second terminal connected to the positive terminal.

Claim 19 (new). A method for operating the device according to claim 11, which comprises the steps of:

performing an operation in a self-controlled manner, which includes the steps of:

putting the switching transistor in a conducting state upon receiving the external control signal and upon a voltage at the secondary winding of the flyback transformer lying beneath a first predefined value;

putting the switching transistor in a nonconducting state if a current flowing through the primary winding of the flyback transformer reaches a second predefined value; and

maintaining the switching transistor in the nonconducting state as long as the voltage at the secondary winding of the flyback transformer exceeds the first predefined value or the external control signal is no longer present.

Claim 20 (new). A method for operating the device according to claim 11, which comprises the steps:

measuring a first signal duration, corresponding to a charging time, at the output of the first voltage comparator;

measuring a second signal duration, corresponding to a discharging time of the flyback transformer, at the output of the second voltage comparator;

comparing each of the first signal duration and the second signal duration with an upper and a lower limit value in the monitoring circuit;

determining that the double layer capacitor and the device for equalizing the charge are in a perfect state as long as the first and second signal durations lie within the upper and lower limit values; and

outputting, through the monitoring circuit, the status signal indicating a presence of the perfect state.

Claim 21 (new). The method according to claim 20, which further comprises:

measuring an amplitude of a rectified discharging voltage, being measured after a transient reaction;

comparing the amplitude with an upper and a lower limit value in the monitoring circuit;

determining that the double layer capacitor is in the perfect state as long as the amplitude lies within the upper and lower limit values; and

outputting from the monitoring circuit the status signal indicating a presence of the perfect state.

Claim 22 (new). A method for operating the device according to claim 11, which comprises the steps:

measuring an amplitude of a rectified discharging voltage, during a discharging operation of the flyback transformer after a transient reaction, the amplitude being proportional to a currently lowest voltage of the single capacitor of the double layer capacitor.

Claim 23 (new). The method according to claim 22, which further comprises:

comparing the amplitude with an upper and a lower limit value

in the monitoring circuit;

determining that the double layer capacitor is in a perfect state as long as the amplitude lies within the upper and lower limit values; and

outputting from the monitoring circuit the status signal indicating a presence of the perfect state.

Claim 24 (new). A method for operating the device according to claim 15, which comprises the steps of:

performing an operation in a self-controlled manner, which includes the steps of:

putting the switching transistor in a conducting state upon receiving the external control signal and upon a voltage at the inductor lying beneath a first predefined value;

putting the switching transistor in a nonconducting state if a current flowing through the primary winding of the inductor reaches a second predefined value; and

maintaining the switching transistor in the nonconducting state as long as the voltage at the inductor exceeds the first predefined value or the external control signal is no longer present.

Claim 25 (new). A method for operating the device according to claim 15, which comprises the steps:

measuring a first signal duration, corresponding to a charging time, at the output of the first voltage comparator;

measuring a second signal duration, corresponding to a discharging time of the inductor, at the output of the second voltage comparator;

comparing each of the first signal duration and the second signal duration with an upper and a lower limit value in the monitoring circuit;

determining that the double layer capacitor and the device for equalizing the charge are in a perfect state as long as the first and second signal durations lie within the upper and lower limit values; and

outputting, through the monitoring circuit, the status signal identify a presence of the perfect state.

Claim 26 (new). The method according to claim 25, which further comprises:

measuring an amplitude of a rectified discharging voltage, being measured after a transient reaction;

comparing the amplitude with an upper and a lower limit value

in the monitoring circuit;

determining that the double layer capacitor is in the perfect state as long as the amplitude lies within the upper and lower limit values; and

outputting from the monitoring circuit the status signal identifying a presence of the perfect state.

Claim 27 (new). A method for operating the device according to claim 15, which comprises the steps:

measuring an amplitude of a rectified discharging voltage, during a discharging operation of the inductor after a transient reaction, the amplitude being proportional to a currently lowest voltage of a single capacitor of the double layer capacitor.

Claim 28 (new). The method according to claim 27, which further comprises:

comparing the amplitude with an upper and a lower limit value in the monitoring circuit;

determining that the double layer capacitor is in the perfect state as long as the amplitude lies within the upper and lower limit values; and

outputting from the monitoring circuit the status signal

indicating a presence of the perfect state.